M4096 SERIES

Power Supply Data Sheet

3U VPX 270V 800W SOSA Aligned

Key improvements over the M4094:
Improved Efficiency
Output Sequencing
SOSA Drivers Compatibility
Upgraded 46.11 Protocol (Compatible IPMITOOL, ELMA ChM)
In-Field Secured programming
Two Level ESD protection

DC/DC POWER SUPPLY

PRODUCT HIGHLIGHTS

- **VITA 62.2 COMPLIANT**
- **SOSA™ ALIGNED**
- **3U FORM FACTOR**
- **UP TO 800 W**
- **OPERATING TEMP: –55°C to +85°C**
- **EMI: Compliant to MIL-STD-461G**
- **Environmental: MIL-STD-810**
- **Input Options:**
  - **MIL-STD-704**
- **Cyber secure**

Table of Contents

1. Scope

The M4096 Power supply is a member of Enercon SOSA Aligned VPX product line and is intended to serve at High Input DC line Input to support a total of 800W steady state, under all Line and temperature conditions.

2. Module High Level Specification Details

Enercon Part Number **M4096-1**

Parameter	Functionality
Form factor	3U VPX, VITA 65 compliant 1: pitch
Cooling	Conduction cooled
Power input	270V Line, Mil-STD-704
Power output	12V/64A, 3.3V/30A, 800W
Management	Tier-II IPMI/46.11 via P0 IPMI-A and IPMI-B (I2C level) ports FPGA based management (JTAG USB is on board)
Temperature	-55C – 85C, conduction cooled
Weight	Approx 800g

2.1 Special Features

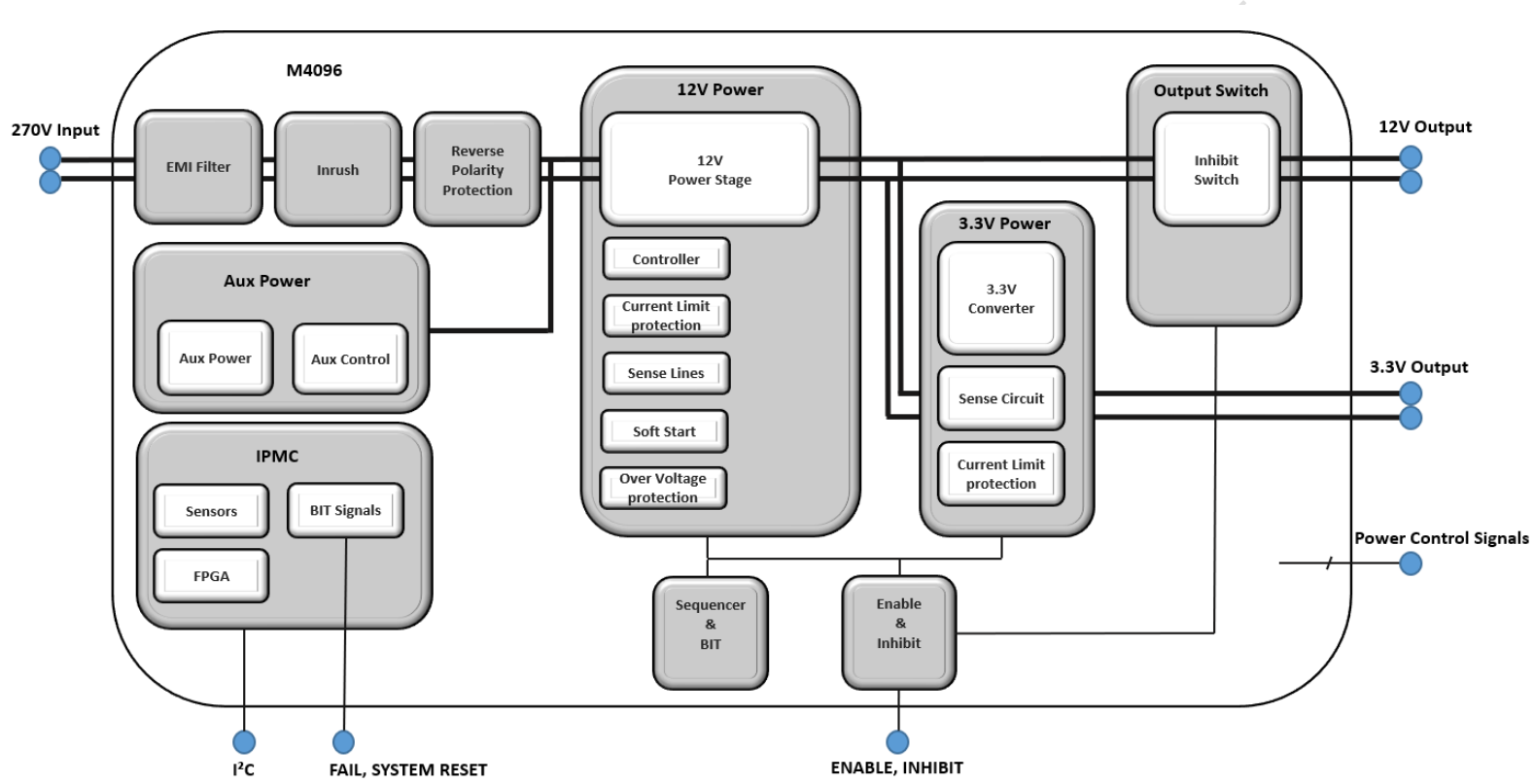
- VITA 62.2
- Aligned with the SOSATM Technical Standard
- ESD Protection
- Wide Input Range
- VITA 62.2 connectors for increased Breakdown Voltage
- Up to 800W output power without derating
- Active Current share
- Remote sense
- Outputs Short Circuit Protection
- Outputs Over Voltage Protection
- Over Temperature Shutdown with Auto Recovery
- Design for Mil-STD-461-G

- System Management: protocol per VITA 46.11 (IPMI Tool, ELMA ChM)

3. M4096 Power Supply Operation

3.1 Unit Block Diagram

M4096 detailed block diagram:



3.2 Electrical Specification

DC Input:

- works through Mil-STD-704 (A-F) Normal and Abnormal Steady State.
- works through Mil-STD-704 (A, E) Normal transients.
- Protected Mil-STD-704 (B, D, E) Normal / Abnormal transients.
- Protected Mil-STD-704 (E, F) Abnormal transients.
- Other Options Available

DC Outputs:

- VS1: 12V / 64A
- 3.3Vaux: 3.3V / 30A

Isolation:

- 500V Input to chassis.
- 500V Input to Output
- 100V Output to chassis

Line Load Regulation

- 12V Output 11.85V to 12.15V
- 3.3V Output 3.28V to 3.52V, 3.25V to 3.45V parallel, PCS.

Efficiency

Up to 92%, Typical.

EMC

Mil-STD-461G:
CE101, CE102, CS101, CS114, CS114, CS115, CS116

Ripple and Noise

Typical less than 50mV (max 1%).
Measured on load after 1 foot harness across 0.1µF capacitor with 10 µF on Load.

System Management Options:

- Simplified IPMI
- IPMC Tier 2

Typical Quiescent Current

- Inhibited Output 20mA (3.3Vaux only).
- Disabled Outputs 17mA (Outputs Off).

Load Transients

Outputs dynamic response less than 5% for Load steps 60% - 90%.
Outputs returns to regulation <1mSec.

3.3 Environmental Specification

Designed for Mil-STD-810G

Temperature:
- Operational -55C° to 85C°
- Exceed Vita 47 CC4.
- Storage -55C° to 125C°
- Designed to meet 600 Thermal Cycles
  Note: Plug-in unit edge surface temperature is measured on the plug-in unit

Altitude:
Method 500.5 procedure I & II
- Storage / Air Transport: 40kft
- Operation / Air carriage: 70kft

Rapid Decompression
Designed to meet per Vita 47.1

Corrosion Resistance
- Mil-STD-810G, Method 509.5.
- VITA47 Class SL1 TBD
- VITA47 Class SL2 TBD

Fungus
Does not support Fungus growth per Mil-HDBK-454, Guideline 4.

Humidity
- Mil-STD-810G, Method 507, up to 95% RH.
- 100% condensation, consult factory.

Vibration & Shock
- Vita47 Vibration Class V1.
- Vita 47 Operational Shock Class OS2
- Vita 47 Bench Handling Shock

ESD
Designed to meet per VITA 47.1

Reliability
375,135 Hours,
calculated IAW MIL-HDBK-217F Notice 2
at +65 ℃, GF

ESS
Environmental Stress Screening available, please contact factory for details

3.4 Unit Interfaces

3.4.1 Connectors

Front Panel Connector **Mating Connector**	TE 2313442-1 or equivalent TE 2313441-1 or equivalent	Main Connector Backplane Connector
Wedge Locks	WAVETHERM SW7-475-250-300-6332-BA	
Key 1 **Key 2**	1-1469492-8 or equivalent 1-2000713-4 or equivalent	315° 135°
Back Panel USB-C Port	USB Type-C	FPGA Programing Port

3.4.2 Functions and Signals

Signal Name	Type	Description
FAIL*	Output Open Drain	Indicates to other modules in the system that a failure has occurred in one of the outputs. [1] [2]
SYSRESET*	Output Open Drain.	Indicates to other modules in the system that an output voltage is not in its nominal range. [1] [2]
INHIBIT*	Input	Controls 12V Output. [1]
ENABLE*	Input	Controls 12V, 3.3V Outputs. [1]
GA0*, GA1*, GA2*	Input	System addressing per VITA46. [1]
SCL_A, SDA_A	buffer	Primary I2C lines. [1]
SCL_B, SDA_B	buffer	Secondary I2C lines. [1]
SYNC IN	Input	Refers to SIGNAL RETURN
PO_SENSE	Output	Output Sense line for voltage compensation. [1]
SENSE RETURN	Output	Output Sense return for voltage compensation. Common line for all outputs.
SHARE	Bi-Directional	Current share pins
3.3V AUX ACS	Bi-Directional	Additional Current share pin to support 3.3VAux Active current share.
SIGNAL RETURUN	Passive	Return path for all signals, refers to Output Power ground.

Notes

1 Refers to SIGNAL RETURN
2 See para for additional information
3 See para for additional information

3.5 Power Detailed Description

3.5.1 Input Voltage

3.5.1.1 Operational Input Range

The M4096 input Voltage range for Mil-STD-704 is per table 3.5.1-1
Unit will be fully operational for all steady state condition and will automatically shut-down when exceeding the Normal Voltage Transient time duration for longer than 1Sec or during Abnormal condition. Protection shut-down would have a minimum 1Sec OFF time.
After shut-down, unit will turn on when input voltage is back to normal steady state.
When applying Input voltage, Unit will turn-on before reaching steady state voltage.

Condition	704A	704B	704C	704D	704E	704F
Steady state	Operational	Operational	Operational	Operational	Operational	Operational
Normal Transients	N/A	Protected	Protected	Protected	Operational	Operational
Abnormal Transients	N/A	Protected	Protected	Protected	Protected	Protected
Reverse Polarity	N/A	Protected	Protected	Protected	Protected	Protected

Table 3.5.1.1-1 Operational Range

Note: for extended Input Range, please contact factory.

3.5.1.2 Transient Response

Power supply is designed to have a good transient response for input voltage transient
An Example of 704F QQ and RR transient under full load is given below

Combined Transient					
QQ	280 Vdc then	< 1 msec < 1 msec	200 Vdc 330 Vdc	10 msec 20 msec	< 1 msec 20 msec
RR	250 Vdc then	< 1 msec < 1 msec	200 Vdc 330 Vdc	10 msec 20 msec	< 1 msec 33 msec

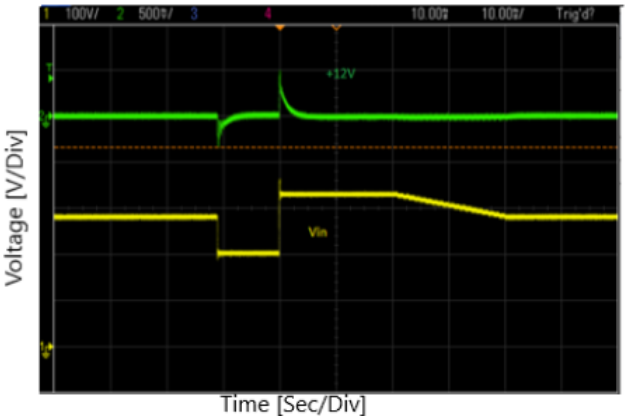


Figure3.5.1-1. 12V response for QQ transient

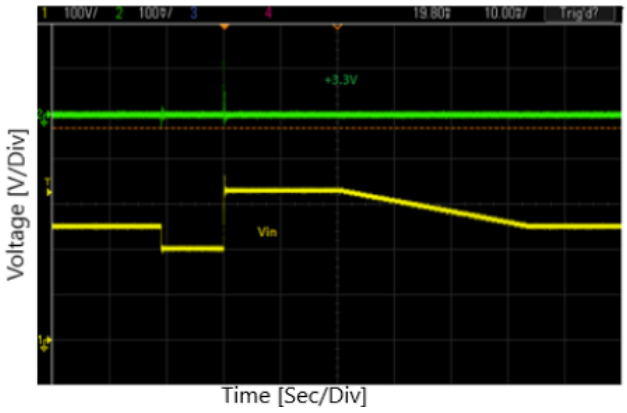


Figure3.5.1-2. 12V response for RR transient

3.5.1.3 Voltage Distortion

Unit verified per Mil-HDBK-704-8 HDC103

System Test							
CONDITION			**LIMITS**				**RESULTS**
270V With Load			+3.3VS2/15A		+12VS1, VS3/64A		
Test	**Frequency**	**Voltage rms**	Vout 3.28V ÷ 3.42V	Ripple ≤ 50mV	Vout 11.85V ÷ 12.15V	Ripple ≤ 120mV	
A	**10Hz**	**0.316**	3.33 V	5 mV	12.00 V	10 mV	Pass
B	**25Hz**	**0.500**	3.33 V	5 mV	12.00 V	10 mV	Pass
C	**50Hz**	**0.562**	3.33 V	5 mV	12.00 V	10 mV	Pass
D	**60Hz**	**0.775**	3.33 V	5 mV	12.00 V	15 mV	Pass
E	**250Hz**	**1.581**	3.33 V	5 mV	12.00 V	25 mV	Pass
F	**1KHz**	**3.162**	3.33 V	5 mV	12.00 V	35 mV	Pass
J	**1.7KHz**	**3.162**	3.33 V	5 mV	12.00 V	35 mV	Pass
H	**2KHz**	**3.162**	3.33 V	5 mV	12.00 V	35 mV	Pass
I	**5KHz**	**3.162**	3.33 V	5 mV	12.00 V	60 mV	Pass
J	**6.5KHz**	**2.433**	3.33 V	5 mV	12.00 V	90 mV	Pass
K	**10KHz**	**1.581**	3.33 V	5 mV	12.00 V	20 mV	Pass

3.5.1.4 Input Redundancy

M4096 can support parallel operation while fed from two independence power sources.
please note: this configuration does not guarantee output redundancy.

3.5.1.5 Input Voltage Rise Time

There is no limitation on Input voltage rise time, contactor or Hot-connection is supported.

3.5.1.6 Inrush Currents

Turn-on inrush current can be divided into 3 categories:
EMI Filter charge Inrush, input current is a function of input voltage rise time charging the EMI filter capacitance. Current limited by setup, typical duration would be a few µSec.
Bus charge Inrush, charging Bus capacitance, controlled by the Unit Inrush circuit with Typical current lower than 3A with a duration of about 3mSec.
Turn-on Inrush, Input current while outputs turn on, typical lower than 1A.

3.5.2 Outputs

3.5.2.1 Outputs Controls: Enable & Inhibit Signals

Outputs are controlled by Enable and Inhibit Signals per VITA 62 definition. See Table 3.5.2.1-1

INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
12V Output	OFF	OFF	ON	OFF
3.3V Aux Output	ON	OFF	ON	OFF

Table 3.5.1.1-1 Outputs Truth table per Signal Status

3.5.2.2 Output Power

Standard configuration will support 12V/64A and 3.3VAux/20A with 2mF capacitance on each output.
No Power derating is required for current share application.
Note: for extended output capacitance, please contact factory.

3.5.2.3 Voltage regulation and Ripple

Volage regulation and ripple are measured as sense point location and limits are under all operational range (Line, Load, Temperature). Limit is also given for ACS (12V, 3.3Vaux optional) and 3.3VAux PCS.

Voltage is measured at connector output, Sense line shorted to output.

Statues	12V Output Limits	3.3VAux Output Limits
Single Unit	11.85V – 12.15V	3.28V – 3.42V
Current Share (3.3VAux ACS)	11.85V – 12.15V	3.28V – 3.42V
Current Share (3.3VAux PCS)	11.85V – 12.15V	3.25V – 3.45V

Table 3.5.1.2-1 Outputs Voltage Regulation under all Line, Load and Temperature
Note: limits above are under all Line, Load and Temperature steady state condition

Ripple is measured at connector output on 0.1µ (20MHz BW)

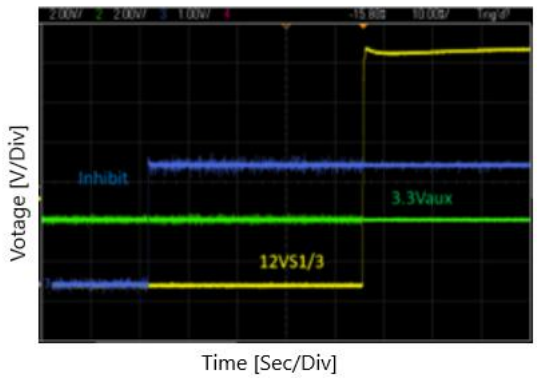
Statues	12V Output Limits	3.3VAux Output Limits
Single Unit	120mV	50mV
Current Share (3.3VAux ACS)	120mV	50mV
Current Share (3.3VAux PCS)	120mV	50mV

Table 3.5.1.2-2 Outputs Voltage Ripple under all Line, Load and Temperature
Note: limits above are under all Line, Load and Temperature steady state condition

3.5.2.4 Turn-on & Sequencing

Unit can support sequencing between 12V and 3.3Vaux, standard configuration would have the 3.3Vaux Turn-on about 50mSec prior to 12V Output.

Typical rise under various condition is given in *Figures 3.5.2.4-1 through 6*



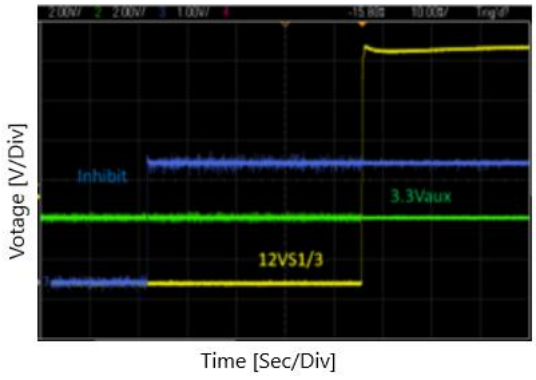
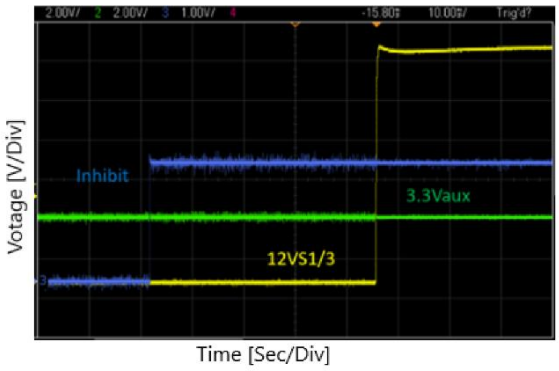


Figure 3.5.2.4-1. 3.3Vaux Inhibit Turn-on



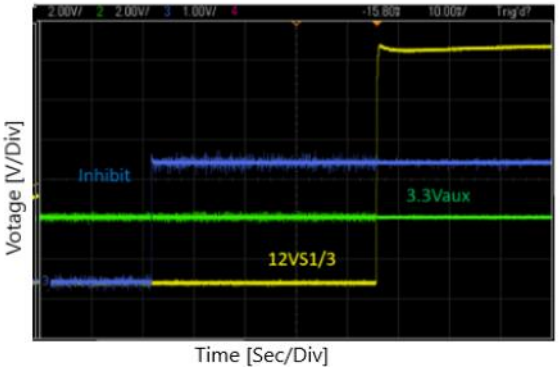


Figure3.5.2.4-2. Enable Turn-on, 12V first

3.5.2.5 Sense Connection

Sense lines are provided for 12V and 3.3Vaux outputs for line voltage drop. Each output has its own sense line with a single SENSE RETURN signal. Recommended connection shown on *Figure 3.5.2.5-1 A8, C8 are redundant 12V Sense lines, B8 is the 3.3Vaux Sense line and D8 is the common-sense return.*

Unit sense circuit can compensate up to 0.4V at full load

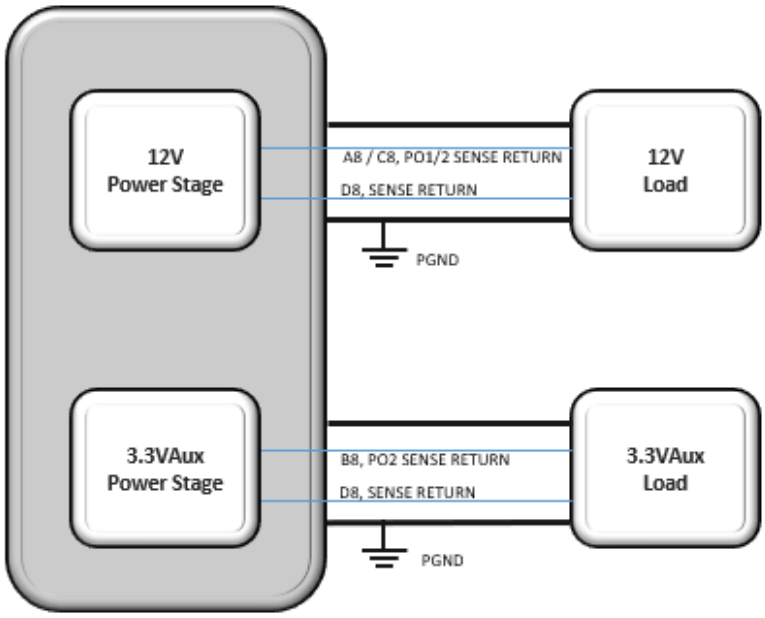


Figure 3.5.2.5-1. Output's sense connection

3.5.2.6 Dynamic Response

Typical performance of a 60% to 90% load dynamic response (need a new one for 3.3V)

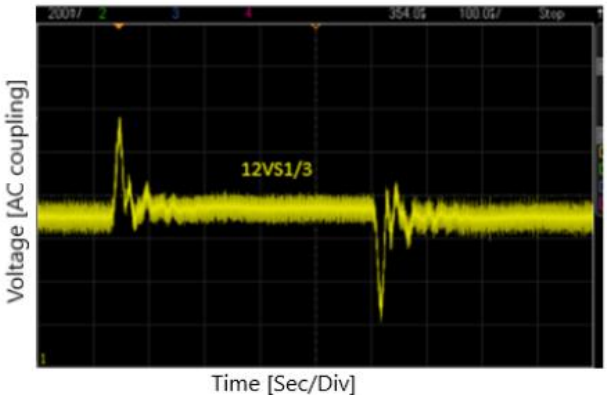


Figure3.5.2.6-1. 12V Dynamic Response

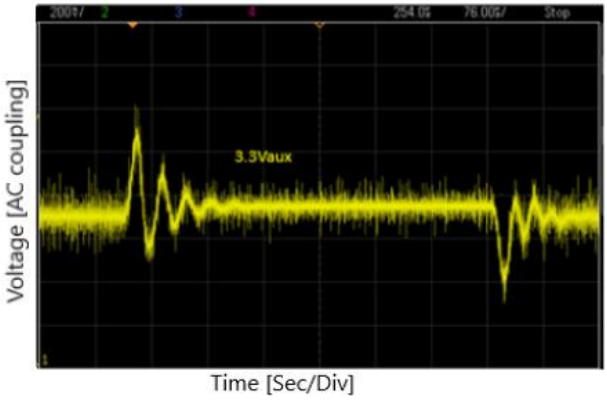


Figure3.5.2.6-2. 3.3V Dynamic Response

3.5.2.7 Current Share

Current share allows the user to connect two or more M4096 units in parallel for doubling the output power of each rail. No derating is required for current share configuration.
Current share typically provides up to 1-3A balance between unit.
An example of 3 M4096 units, each providing about 50A can be shown on
Figures *3.5.2.7-1 through 2.*

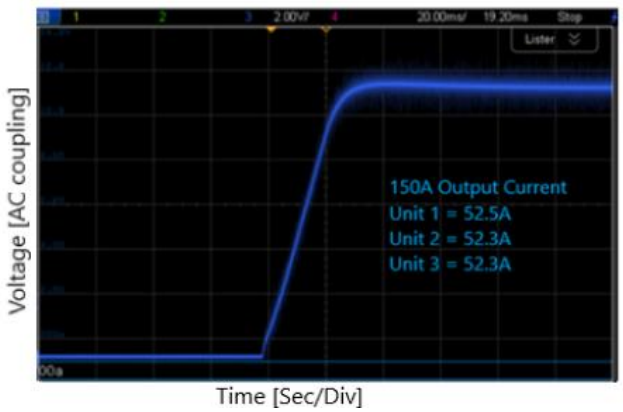


Figure 3.5.2.7-1 (3 units) current share Turn-on

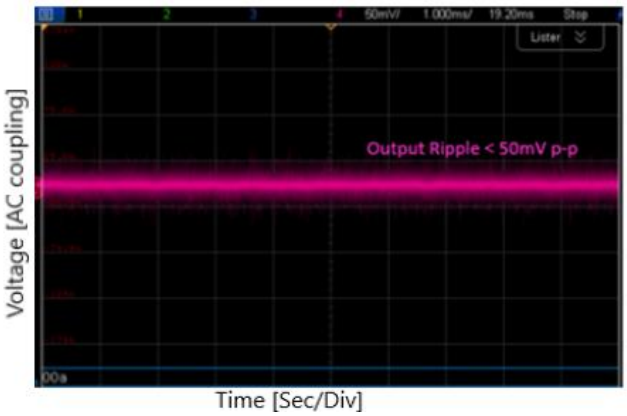


Figure 3.5.2.7-2 (3 units) Output Ripple

12V output is using Active Current Share topology. By comparing the actual current between paralleled units, the unit can provide accurate share balance between outputs with very low susceptibility to power traces and sense connection and no need for voltage drop.
The 3.3Vaux output supports both Passive Current share with voltage drop or ACS with an additional U.D pin.
During a fault condition for both ACS or PCB, both relative outputs will hiccup synchronously to support synchronous turn on into load.
Typical current share connection is given on *Figure 3.5.2.7-3*

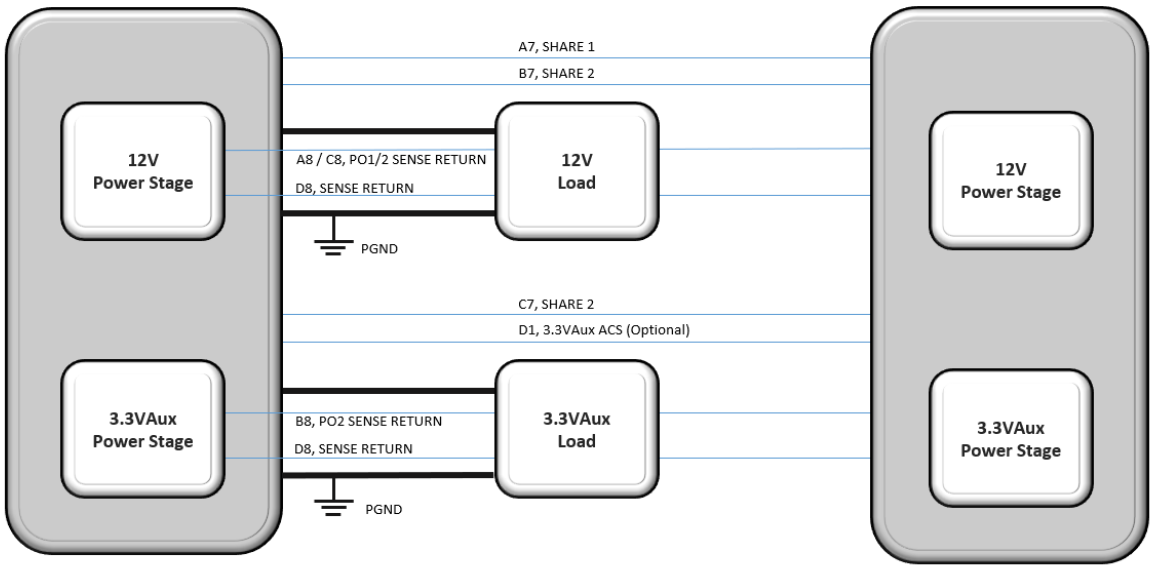


Figure 3.5.2.7-3 current share connection.

Note: For best current share balance, make sure both outputs SENSE lines are connected to a single load point to insure Vout each outputs is as close as possible to the other.

Please note:

- Current share is an optional configuration
- Typically, current share starts at load above 10% of max load
- No derating is required
- Current share is not a guarantee for redundancy, some failures (E.g. short on output) will result in a failure of both units.
- During Over load condition, both relative outputs will be synchronized with their hiccup to allow Turn-on into full load once the fault condition is removed.
- Multiple current share units are optional.

3.5.2.8 Short Protection

Both 12V and 3.3VAux outputs have an indefinite hiccup for over-Load / short circuit protection. The over-load hiccup threshold is 110%-120% of nominal current. Output will automatically recover after removal of fault condition.
A short on 3.3VAux rail will not affect the 12V Output, a short on the 12V rail will cause the 3.3VAux to hiccup as well.
While output is at hiccup mode, current during on-time may exceed 140% of max current

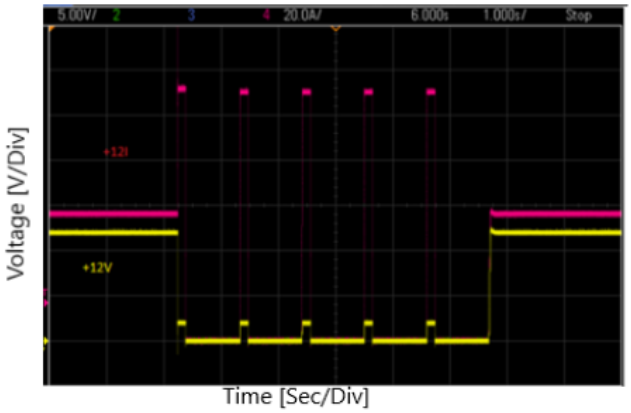


Figure 3.5.2.8-1 12V Output hiccup and recovery after short

3.5.3 Signals

3.5.3.1 Fail bit & SYSTEM RESET

Unit has two dedicate Fault signals:

Fail BIT: Indicates that one of the power supply outputs is out of its range, in respect to the expected value depending on Inhibit & Enable status.

Open drain output (Per VITA 65), Normally Open and goes Low during Fail event.

SYSTEM RESET: Indicates that one of the power supply outputs is out of its nominal range.

Open drain output (Per VITA 65), Normally Open and goes Low when output is out of nominal range.

Note: for the M4096 this BIT standard configuration is as "Output".

Fail BIT & SYSTEM RESET responses under different conditions are given under Figures 3.5.3.1-1 to 5.

Note: Test setup for BITs condition have external 3.3V pullup (not unit's 3.3VAux).

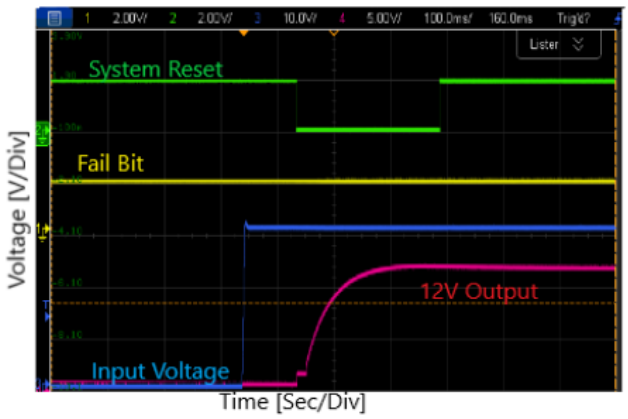


Figure 3.5.3.1-1 BITs status during Input voltage Turn-o

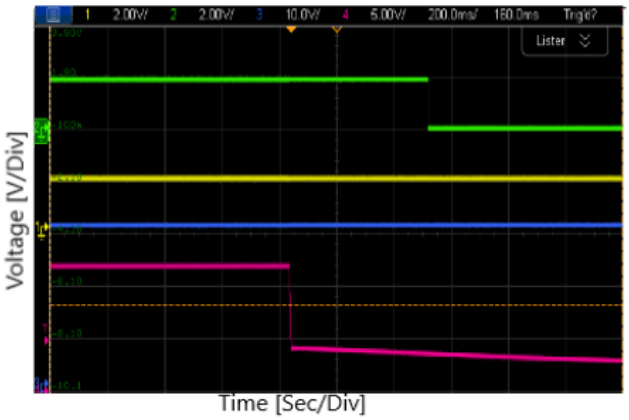


Figure 3.5.3.2-2 BITs status Enable Turn-off

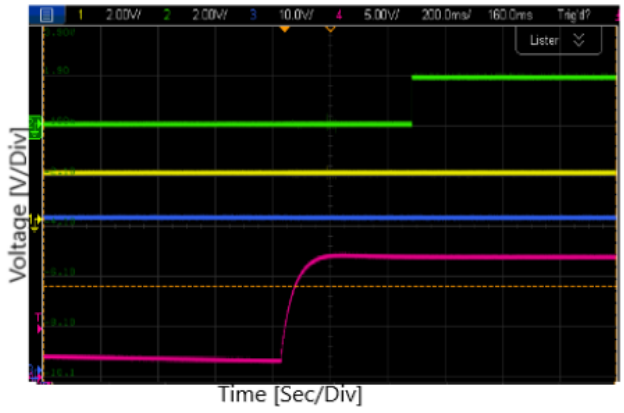


Figure 3.5.3.2-3 BITs status Enable Turn-on

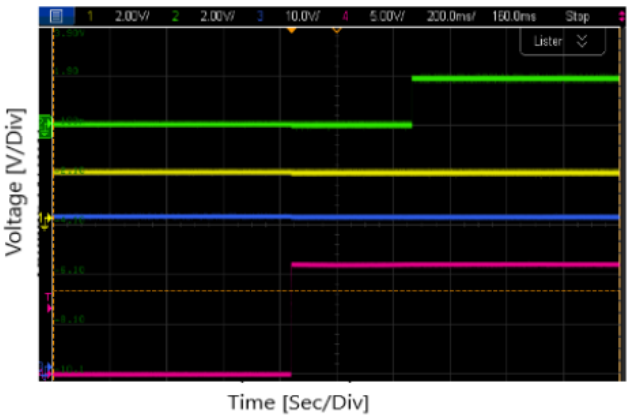


Figure 3.5.3.2-4 BITs status Inhibit Turn-on

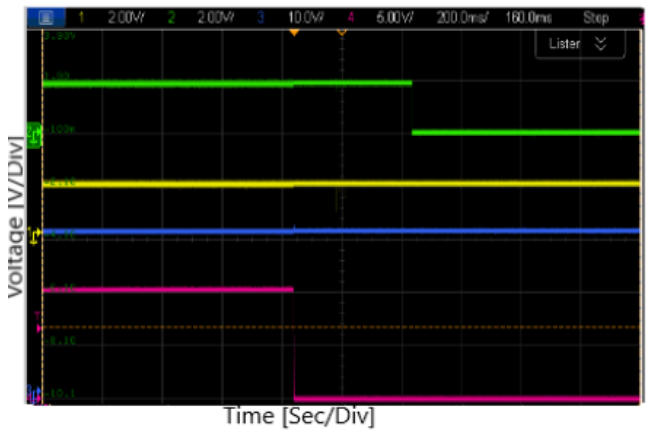


Figure 3.5.3.2-5 BITs status Inhibit Turn-off

3.5.3.2 SYNC IN

Pin can be used to synchronize the power supply switching frequency to an external clock. Standard switching frequency with no Sync In signal applied is 120KHz input stage / 220kHz ±5% Output Stage. When configured to use Sync, the unit will sync to a signal between 200kHz and 300kHz ±5%. The square wave must be at 3.3V CMOS standard logic levels with a duty cycle between 20% and 80%. The M4096 will sync after 32 cycles within tolerance of external clock. The unit will revert to its internal clock frequency upon any out of specification clock cycles and will need 32 good cycles to resync to the external clock. Contact factory to add Sync_In functionality and to customize its configuration values.

Notes:

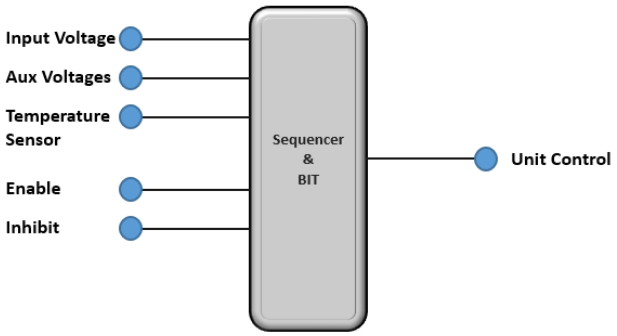
1. Functional is optional, please contact factory.
2. When not used, keep open.
3. Deviating from original frequency may affect efficiency.

3.5.4 Built In Tests

For proper operation, the unit has Built In Test circuit, which continuously monitors Unit's internal functions, such as: Input Voltage, Internal Aux voltage, Temperature, Output voltages and control proper Turn-on and Turn-off Sequence.

Turn on: verification that all parameters are withing proper and all Aux voltage are stabilize before starting outputs Turn-on sequence.

Continues: Monitoring all critical parameters and initiating a controlled Turn-off sequence when required.



3.5.5 Thermal Management

Operational Temperature range is -55°C to +85°C on the surface of the edge that contacts the rack/enclosure. The contacting surface on the rack need to be at lower temperature to account for thermal resistance between the unit and the chassis/cold plate. The M4096 wedge locks are defined as 0.1 °C/W Resistance per Card Edge. The thermal design of the unit will provide a balanced power dissipation between both sides of the unit.
The unit has two thermal sensors.
I2C thermal sensor for 46.11.
Analog Thermal Sensor for protection and shutdown. Shutdown temperature would be between 90°C to 105°C at unit edge, load depended.
No power derating is required for all operational temperature range

3.5.6 Efficiency

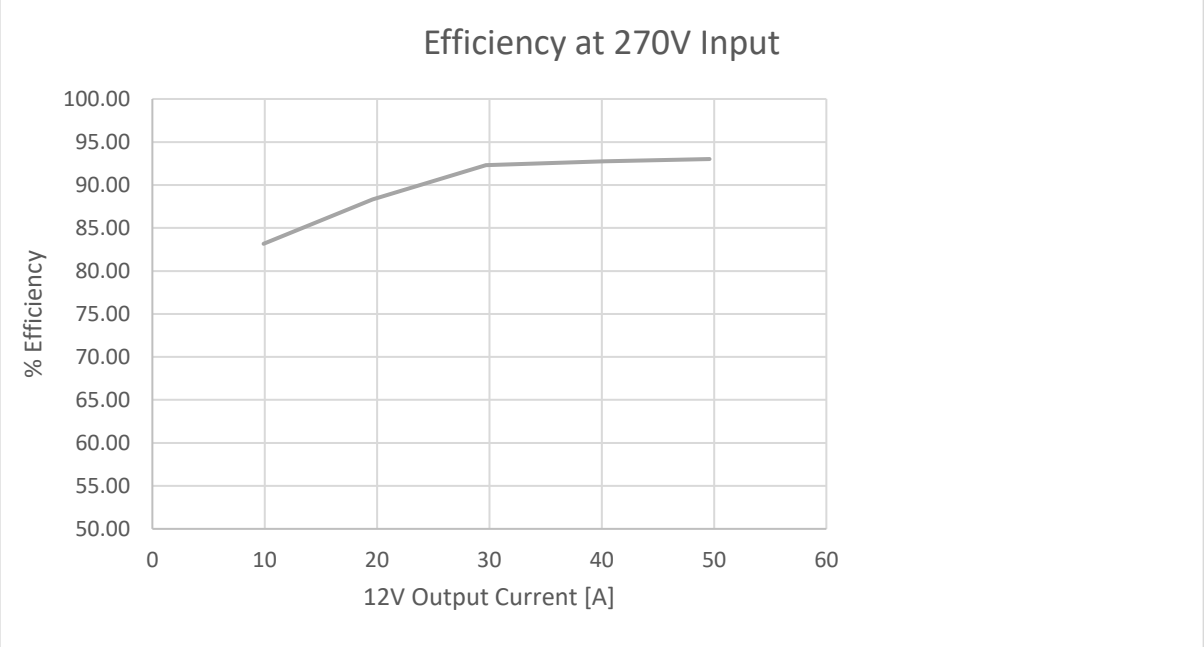


Figure 3.6-1. Typical efficiency, room temperature

3.5.7 EMI

EMI Test per Mil-STD-461G for CE101, CE102

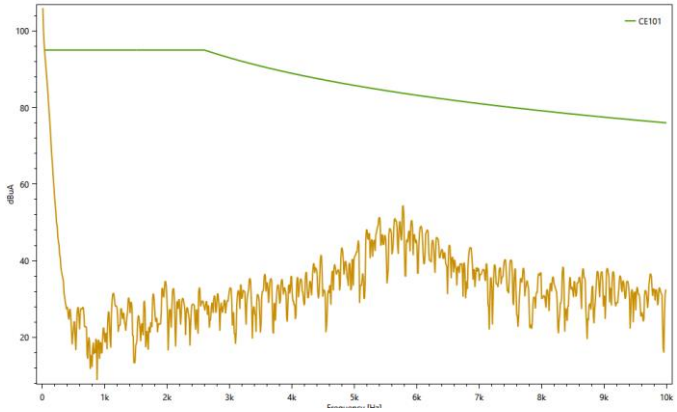


Figure 3.5.7-1. CE101 Full Load

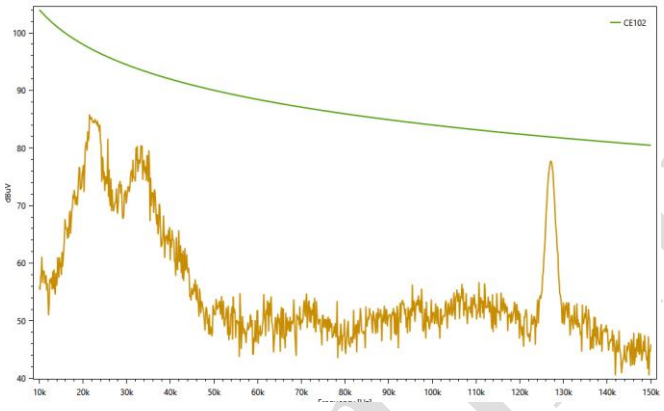


Figure 3.5.7-2. CE102 Full Load, 10KHZ to 150KHZ

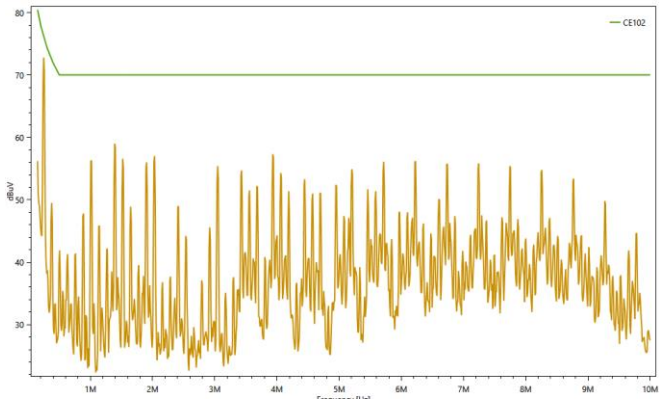


Figure 3.5.7-3. CE102 Full Load, 150KHZ to 10MHZ

3.6 System Management

3.6.1 Electrical Interface

I²C Buffers	LTC4300
Pullups	20KΩ
Vcc	3.3V
USB-C Port	Jedec Programing

3.6.2 Communication Protocol

The M4096 can be configured to one of the two I2C communication protocols: 46.11 Tier 2 IPMC or Simplified I2C.
Slot location, for both options, is defined per VITA62. See table 3.7.2-1.
There following data Sensors are available:
Output Current sensors: Max error of +/-5% or up to +/-1A (the bigger of the two)
Output Voltage sensors: Max error up to +/-0.2V
Input Voltage sensors: Max error up to +/-0.5V
Temperature sensors: ±5C (Internal measurement).

Slot Number	A6	A5	A4	A3	A2/GA2*	A1/GA1*	A0/GA0*	Hardware Address
Slot0	0	1	0	0	0 / U	0 / U	0 / U	20
Slot1	0	1	0	0	0 / U	0 / U	1 / G	21
Slot2	0	1	0	0	0 / U	1 / G	0 / U	23
Slot3	0	1	0	0	0 / U	1 / G	1 / G	24

Table 3.7.2-1 Address Space
Note: A0÷A6 represent Firmware address and GAx represent the physical Geographical Address.
U = Unconnected; signal is pulled-up on the unit and result as logic "0"
G = Biased to Ground on the Backplane; results in a logical "1"

3.6.2.1 IPMC, 46.11 Tier2

The M4096 design to support both ELMA's ChM and IPMITOOL System Interface. Adjustments can be made to support custom ChM configurations.

Sensor ID	Sensor Type	Name
00	F0h	FRU State Sensor
01	F1h	System IPMB Link Sensor
02	F2h	FRU Health Sensor
03	02h	FRU Voltage Sensor
04	F3h	FRU Temperature Sensor
05	F4h	Payload Test Results Sensor
06	F5h	Payload Test Status Sensor
07	02h	VS1 Voltage
08	03h	VS1 Current
09	02h	VS2 Voltage
10	03h	VS2 Current
11	01h	Analog Temperature
12	02h	Input Voltage
N/A	N/A	Device Locator Record
N/A	N/A	Device Management

Table 3.6.2.1-1. Sensor Allocation

IPMITOOL Command
SDR List
Sensor List
Fru Print
SEL List
SEL Clear

Table 3.7.2.1-2. Supported *IPMITOOL* Commands

IPMI Command	NetFn	Group ID	CMD
Get Device ID	APP	N/A	01h
Get Self-Test Results	APP	N/A	04h
Get FRU Inventory Area Info	Storage	N/A	10h
Read FRU Data	Storage	N/A	11h
Set Event Receiver	S/E	N/A	00h
Get Event Receiver	S/E	N/A	01h
Get Device SDR info	S/E	N/A	20h
Get Device SDR	S/E	N/A	21h
Reserve Device SDR Repository	S/E	N/A	22h
Get Sensor Reading	S/E	N/A	2Dh
Get VSO Capabilities	Group Extension	VSO (03h)	00h
Set IPMB State	Group Extension	VSO (03h)	09h
Get Device Locator Record ID	Group Extension	VSO (03h)	0Dh
Fru Control Capabilities	Group Extension	VSO (03h)	1Eh
Get FRU Address Info	Group Extension	VSO (03h)	40h

Table 3.7.2.1-3. Supported *RAW IPMI* Commands

Sensor Name	Parameter	Upper Non-Recoverable Threshold	Upper Critical Threshold	Upper Non-Critical Threshold	Lower Non-Critical Threshold	Lower Critical Threshold	Lower Non-Recoverable Threshold
VS1 12V	Voltage	13V	12.8V	12.6V	11.6V	11.4V	11.2V
	Current	74A	70A	64A			
3.3VAux	Voltage	4.2V	4.0V	3.8V	3V	2.8V	2.6V
	Current	24A	22A	20A			
Temperature	Temperature	95°C	90°C	85°C	-55°C	-60°C	-60°C
Vin	Voltage	340V	290V	280V	250V	240V	190V

Table 3.7.2.1-4. Sensors Thresholds

Note: Thresholds level can be updated by request.

3.6.2.2 Simplified I2C Communication

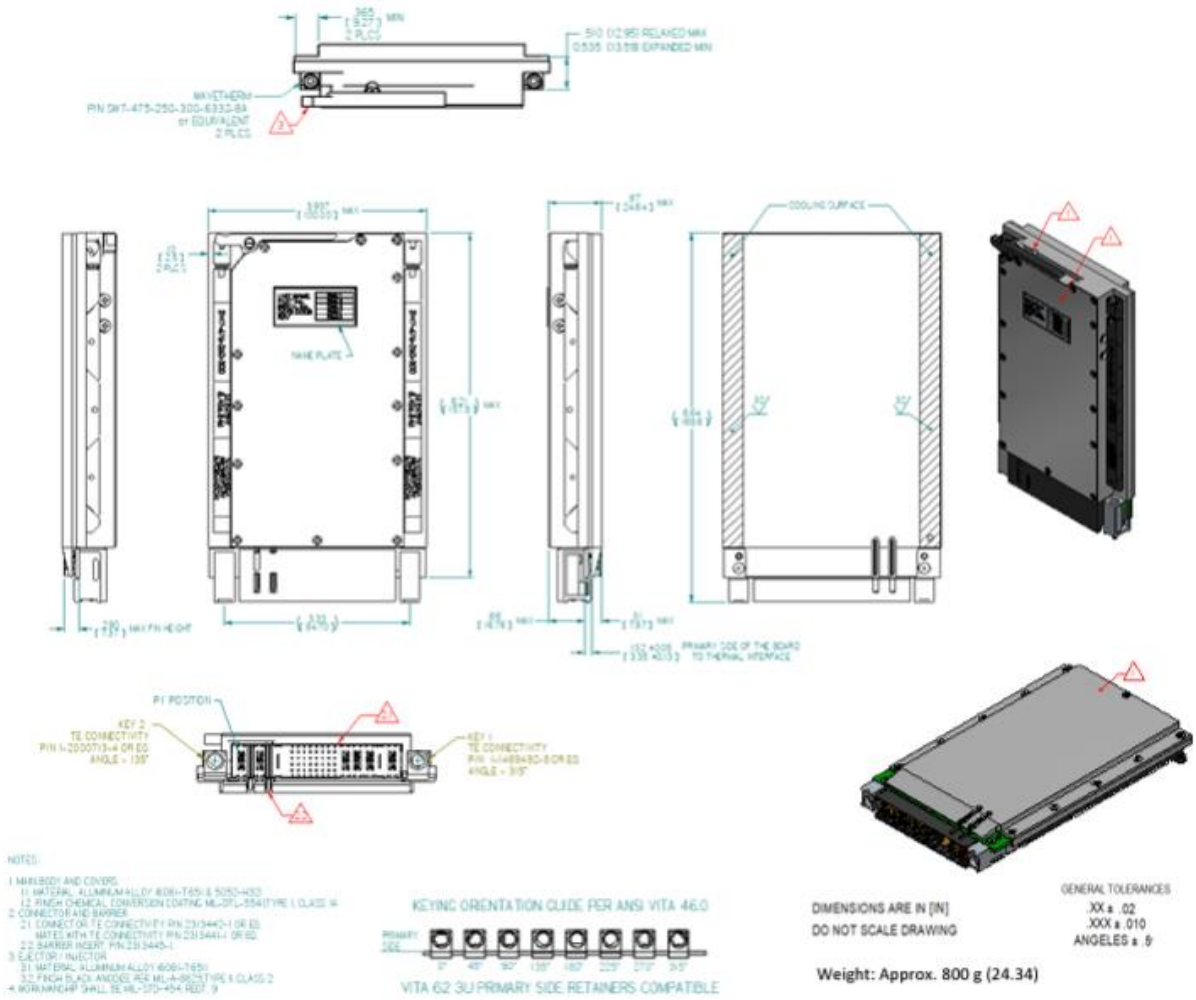
This communication protocol serves as an option when 46.11 compatible ChM is not use.

Response Byte #	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		21 Hex
1		N/A		00 Hex
2-3	S Integer, MSB First	Temperature -55C to 120C	T(C°)=+/- 7bit Dec	-55°C to 125°C
4-5	U Integer, MSB First	12V VS1 Voltage	V(out) = Data· m2	20.48V
6-7	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data· m2	20.48V
8-9	U Integer, MSB First	N/A	N/A	N/A
10-11	U Integer, MSB First	N/A	N/A	N/A
12-13	U Integer, MSB First	N/A	N/A	N/A
14-15	U Integer, MSB First	N/A	N/A	N/A
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data· m3	80A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data· m3	20A
20-21	U Integer, MSB First	N/A	N/A	N/A
22-23	U Integer, MSB First	N/A	N/A	N/A
24-35	U Integer, MSB First	N/A	N/A	N/A
26-27	U Integer, MSB First	N/A	N/A	N/A
28-29	U Integer, MSB First	Reserved	00Hex	
30-31	U Integer, MSB First	Reserved	00Hex	
32-51	Character String (ASCII)	Part Number	M4094-xxx* (Note1)	20 Characters
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec (Note2)	Optional
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec (Note2)	Optional
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	Optional
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (Note4)	2 Characters
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	4 digits
62	U Integer, MSB First	Reserved		AA Hex
63	U Integer, MSB First	Zero Checksum	Value required to make the sum of bytes 0 to 62 added to a multiple of 256	

3.7 Pinout

Pin Number	Pin Name (12V Only)	Function
P1	-DC_IN/ACN	270V Return
P2	+DC_IN/ACL	270V
LP1	CHASSIS	CHASSIS
P3	+12VDC (Vs1)	12V Output
P4	POWER_RETURN	Input Return
P5	POWER_RETURN	Input Return
LP2	3.3V_AUX	3.3V Output
P6	+12VDC (Vs1)	12V Output
A8	SENSE, +12VDC	12V Sense
B8	SENSE, 3.3V_AUX	3.3V Sense
C8	SENSE, +12VDC	12V Sense
D8	SENSE_RETURN	Sense Return
A7	SHARE_1	Current Share 1
B7	SHARE_2	Current Share 2
C7	SHARE_3	Current Share 2
D7	SIGNAL RETURN	Signal Return
A6	SM2	I^2C SCL B
B6	SM3	I^2C SDA B
C6	N Reserved C.	D.N.C.
D6	SYSRESET*	SYSRESET*
A5	GA0*	GA0*
B5	GA1*	GA1*
C5	SM0	I^2C SCL A
D5	SM1	I^2C SDA A
A4	Reserved	D.N.C.
B4	Reserved	D.N.C.
C4	Reserved	D.N.C.
D4	Reserved	D.N.C.
A3	SYNC_IN (UD0)	External Sync Clock
B3	Reserved	D.N.C.
C3	NED	D.N.C.
D3	NED RETURN	D.N.C.
A2	VBAT	D.N.C.
B2	FAIL*	FAIL*
C2	INHIBIT*	INHIBIT*
D2	ENABLE*	ENABLE*
A1	SYNC_OUT (UD1)	D.N.C.
B1	NVMRO (UD2)	D.N.C.
C1	GA2* (UD3)	GA2
D1	UD4	3.3V ACS

3.8 Mechanical SCD



*** Specifications are subject to change without prior notice by the manufacturer.**

Appendix A – VITA 47 Compliance (For full compliance please contact Factory)

A.1 Environmental

A.2 Design

A.3 Safety

A.4 Quality

Appendix B – Restricted materials